CLAIMS

1. A semiconductor device comprising:

a support substrate;

an embedded insulating layer formed on the support substrate;

a semiconductor layer on the embedded insulating layer;

at least an element region formed in the semiconductor layer;

a plurality of source/drain regions of a first conductivity type, formed in the element region at predetermined intervals;

a plurality of body regions of a second conductivity type, sandwiched between a pair of adjacent ones of the source/drain regions in the element region; and

a gate formed on each of the body regions with a gate insulating film being laid between them,

each of the source/drain regions including:

an inner high-concentration portion extending to the embedded insulating layer, and

an outer low-concentration portion surrounding the inner high-concentration portion and having a direct contact with the body regions.

2. The semiconductor device according to claim 1, wherein the high-concentration portion of the source/drain region includes elements larger in atomic number than those included in the low-concentration portion.

3. The semiconductor device according to claim 1, wherein the semiconductor in the high-concentration portion is in an amorphous state.

4. The semiconductor device according to claim 1, wherein the body region is configured to be able to store a charge developed when current flows between two source/drain regions both sides of the body region.

5. The semiconductor device according to claim 1, wherein each of the source/drain regions includes an upper extension region and a diffusion region smaller in diameter than the upper extension region.

6. The semiconductor device according to claim 1, wherein on each of the source/drain regions, a conductive layer is formed.

7. The semiconductor device according to claim 6, wherein both sides of each of the gates are adjacent to the conductive layers, with a multilayer of an oxide film and a nitride film.

8. A semiconductor device comprising:

a support substrate;

an embedded insulating layer formed on the support substrate; and

a row of element units formed on the embedded insulating layer in a first direction, the element units being isolated from each other by an isolation recess having a predetermined width along the first direction,

each of the element units including:

a pair of source/drain regions of a first conductivity type, opposite to each other along the first direction;

a body region of a second conductivity type, sandwiched between the pair of source/drain regions; and

a gate formed on the body region with a gate insulating film being laid between them, and

the width of the isolation recess being set smaller than that of the element unit itself in a second direction perpendicular to the first direction.

9. The semiconductor device according to claim 8, wherein an insulating film is embedded in the isolation recess.

10. The semiconductor device according to claim 8, wherein a conductive film is embedded in a part of the isolation recess.

11. The semiconductor device according to claim 8, wherein the element unit itself is 0.1 μm or less in width in the second direction.

12. The semiconductor device according to claim 8, wherein a cavity exists in the insulating film embedded in the isolation recess.

13. The semiconductor device according to claim 8, further comprising a plurality of the rows of element units extending in the first direction and being generally parallel to each other, wherein

between each of adjacent two of the rows of the element units, an element isolation region extending in the first direction is formed, and

ones, laid on the same line along the second line, of the isolation recesses in the rows of element units are communicated with each other through recesses formed in the element regions, respectively.

14. The semiconductor device according to claim 8, wherein two source/drain regions adjacent to each other in the first direction in the row of element units are electrically short-circuited to each other.

15. The semiconductor device according to claim 8, wherein the body region in each of the element units is configured to be able to store a charge generated when a current flows through the source/drain regions opposite to each other in the first direction.

16. The semiconductor device according to claim 14, wherein the adjacent two source/drain regions are electrically short-circuited to each other via a contact plug.

17. The semiconductor device according to claim 16, wherein an insulating film is formed between the gate and the contact plug in the element unit.

18. The semiconductor device according to claim 8, wherein each of the source/drain regions includes an upper extension region and a lower diffusion region smaller in diameter than the upper extension region.

19. The semiconductor device according to claim 8, wherein on each of the source/drain regions, a conductive layer is formed.

20. The semiconductor device according to claim 19, wherein both sides of each of the gates are adjacent to the conductive layers, with a multilayer of an oxide film and a nitride film.